Optimization of various isolation techniques to develop low noise, radiation hard double-sided silicon strip detectors for the CBM Silicon Tracking System

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Abstract

This paper reports on the design optimization done for Double Sided silicon microStrip Detectors (DSSDs) to reduce the Equivalent Noise Charge (ENC) and to maximize the breakdown voltage and Charge Collection Efficiency. Various isolation techniques have been explored and a detailed comparison has been studied to optimize the detector performance. For the evaluation of the performance of the silicon detectors, a radiation damage model has been included. The neutron fluence is expected to be 2×10^{13} $n_{eq}cm^{-2}$ per year for five years of expected CBM run with intermediate periods of warm maintenance, cold maintenance and shutdown. Transient simulations have been performed to estimate the charge collection performance of the irradiated detectors and simulations have been verified with experimental data.

Keywords: Double Sided silicon Strip Detector, Equivalent Noise Charge (ENC), radiation hardness, Transient simulation, Charge collection, Strip isolation, TCAD, SYNOPSYS

1. Introduction

The mission of the Compressed Baryonic Matter (CBM) [1] experiment at the Facility for Antiproton and Ion Research (FAIR) now under construction in Darmstadt, Germany, is to explore the QCD phase diagram in the region of high baryon densities. The layout of CBM detectors is driven by the corresponding experimental requirements concerning material budget, reaction rates, radiation tolerance, particle densities and selectivity. The detector will face the problem of measuring Au+Au interactions at 25 GeV/nucleon and up to 10MHz rate producing up to 1000 charged particle tracks per event. The core of the CBM detector is Silicon Tracking Station (STS) located in a large-aperture dipole magnet. The STS of the CBM will consist of eight tracking stations placed at a distance between 10-100 cm downstream of the target in a dipole magnet with internal field of 1 Tm. Each station is a modular structure of DSSDs of different sizes to match the non-uniform channel occupancy distribution from the beam pipe to the periphery. The sensors will be held by low-mass carbon fibre support structures with read-out electronics outside of the detector aperture, thus minimizing the Coulomb scattering of particles.

Table 1: Fluence profile of neutrons expected for CBM STS

Year	Fluence (n_{eq} cm^{-2})	N_{eff} (cm^{-3})	τ_e (ns)	τ_h (ns)	V_{fd} (V)	V_{op} (V)
1	2×10^{13}	2.80×10^{11}	1140	1050	28	70
2	4×10^{13}	-1.54×10^{11}	570	527	20	50
3	6×10^{13}	-5.35×10^{11}	380	351	44	110
4	8×10^{13}	-8.84×10^{11}	285	263	75	150
5	1×10^{14}	-12.1×10^{11}	228	211	100	200

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We aim to develop low-noise radiation hard DSSDs for the CBM STS. This is a challenging task keeping in mind that CBM uses fast self-triggering electronics; the shaping time of the front end chip used for early prototyping [2] is 19 ns (fast shaper) and 140 ns (slow shaper) respectively. The dominant contribution to the total Equivalent Noise Charge (ENC) is given by the series capacitive and the resistive components [3, 4, 5]. These two noise components are further inversely proportional to the shaping time of the preamplifier. The other less significant contributions to the total ENC like shot noise has also been taken into account in this study. Parameters relevant for the extraction of these two dominant components of ENC like interstrip capacitance and metal trace resistance has been studied. The various contributions to the total Equivalent Noise Charge (ENC) are given as follows:
(a) Series Capacitive Noise

$$a + b.C_{tot} \tag{1}$$

(b) Series Resistive Noise

$$24.C_{tot}(pF).\sqrt{R_s(\Omega)/\tau_s(ns)}e^- \tag{2}$$

(c)Shot Noise

$$108.\sqrt{I_{leak}(\mu A).\tau_s(ns)}e^- \tag{3}$$

(d)Parallel Resistive Noise

$$24.\sqrt{\tau_s(ns)/R_p(M\Omega)}e^- \tag{4}$$

where a and b are electrical parameters dependent on the front end electronics, C_{tot} is the total capacitance, R_s is the series resistance, τ_s is the shaping time of the preamplifier, I_{leak} is the leakage current and R_p corresponds to the bias resistor value.

Table 1 shows the expected neutron fluence for five years of expected CBM runtime. The maximum fluence is expected to be 1×10^{14} $n_{eq}cm^{-2}$ which is similar to the Large Hadron Collider (LHC) radiation environment. One can observe a deterioration of carrier life time with fluence which will have an impact on the Charge Collection Efficiency (CCE), especially on the p-side since this side collects less mobile holes. In order to understand radiation damage, some of the CBM prototype DSSDs having dimension 1.6 cm×1.6 cm and resistivity 6 kΩcm were irradiated at the KRI cyclotron facility in St. Petersburg, Russia. These detectors were measured just after irradiation without any periods of annealing. The variation of leakage current and interstrip resistance with neutron fluence has been measured. The radiation damage model implemented in TCAD simulations is able to reproduce the measured observations.

In order to investigate the life time of DSSDs, it is imperative to extract CCE as a function of fluence for which one has to understand strip isolation in particular on the ohmic side. Hence we are exploring various isolation techniques, for example P-stop, P-Spray, Modulated P-spray (conventional isolation techniques) and also a new isolation technique namely, Schottky barrier. TCAD simulations have been performed to optimize the total ENC, strip isolation and to maximize the breakdown voltage (V_{bd}) and CCE. Transient simulations can be used to extract the operating voltage of DSSDs which in turn depends on the isolation technique.

2. Structure of simulated devices

2.1. Simulated structure of DSSD

The AC-coupled DSSDs with n-type silicon substrate of 300 μm thickness have a strip width of 20 μm, a pitch of 50 μm with orthogonal strips, as shown in Figure 1. The n-strips are orthogonal to the p-strips. We are using moderate resistivity n-type silicon of around 5-6 kΩcm corresponding to effective doping concentration of 9×10^{11} cm^{-3} and 7.5×10^{11} cm^{-3}, respectively. All p^+ and n^+ implants were approximated by assuming a Gaussian profile with a peak concentration of 5×10^{19} cm^{-3} at the surface. It is assumed that the lateral diffusion depth at the junction curvature of the implants is equal to 0.8 times the vertical junction depth (X_j). Depletion is attained by applying a positive voltage to the ohmic side and grounding the junction side. The thickness of the coupling oxide taken is around 200 nm while the interstrip gap is filled with a thicker oxide of around 800 nm. The surface oxide charge (Q_f) has been taken to be 3×10^{11} cm^{-2} before irradiation for a good quality oxide. For the $< 111 >$ silicon orientation used in detector fabrication, the amount of charge is expected to increase and saturate at 3×10^{12} cm^{-2}, under heavy irradiation of the

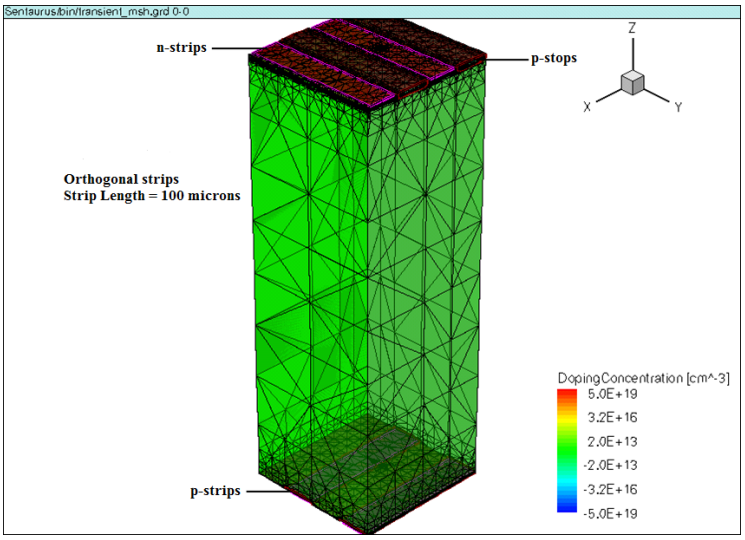

Figure 1: Slice of 3-dimensional DSSD grid having orthogonal strips.

order of a few hundred krad [6, 7]. The conventional isolation techniques namely P-stop, P-spray and Modulated P-spray have been compared with a new isolation technique called Schottky barrier. The TCAD simulation grids having these isolation techniques can be seen in Figure 2(a-d). The conventional isolation techniques have been defined by assuming a Gaussian profile with a peak concentration of 5×10^{19} cm^{-3} at the surface for P-stop and 4×10^{16} cm^{-3} (low dose) for P-spray. For modulated P-spray, an optimization study has been done for various combinations of P-stop width and P-spray dose which will be discussed later in this paper. The new isolation technique namely Schottky barrier can be defined either through metal work function value or through barrier height which in turn depends on the substrate type and the metal used for schottky contact. For Aluminium, the barrier height is 0.72 eV for n-type silicon while for p-type silicon, the barrier height is 0.58 eV [8, 9].

For accurate simulations, it is imperative to use correct boundary conditions. The reason being that we are simulating only a part of a full device, hence we need to be sure that this does not affect the accuracy of the simulation. One possible way to do this is to simulate larger area of the device and then to look at the results only in the central region, away from the boundaries. The other approach is to simulate some repeating unit of device and then to make sure that the boundary conditions are appropriate. The default is to use reflecting (Neumann) boundary conditions for a device with transitional symmetry and mirror symmetry. However in our device with orthogonal strips, there is transitional symmetry in x and y direction but no mirror symmetry. Hence we have applied periodic boundary conditions (PBC) in x and y direction for device having orthogonal strips.

2.2. Models implemented in TCAD simulation

SYNOPSYS [10], a finite element semiconductor simulation package was used to determine the electrical behaviour of these devices. The effective doping concentration (N_{eff}) is parameterized using Hamburg model [11, 12] which consist of three components, a short term beneficial annealing component, a stable damage part and a reverse annealing component. To incorporate the effect of increase in leakage current with fluence, the minority carrier lifetime τ has been changed in our simulation package using the definition of Kraner [13] as follows:

$$1/\tau = 1/\tau_0 + \beta.\phi_{eq} \tag{5}$$

where τ_0 is the minority carrier lifetime of the initial wafer, ϕ_{eq} is the integrated fluence, and β is the trapping time. The default value of τ_0 for the electrons and holes is 10 μs and 3 μs in Sentaurus Device. These values have been modified in Scharfetter relation [14] to a value of 1 ms for electrons and 0.3 ms for holes as is expected for detector grade silicon.

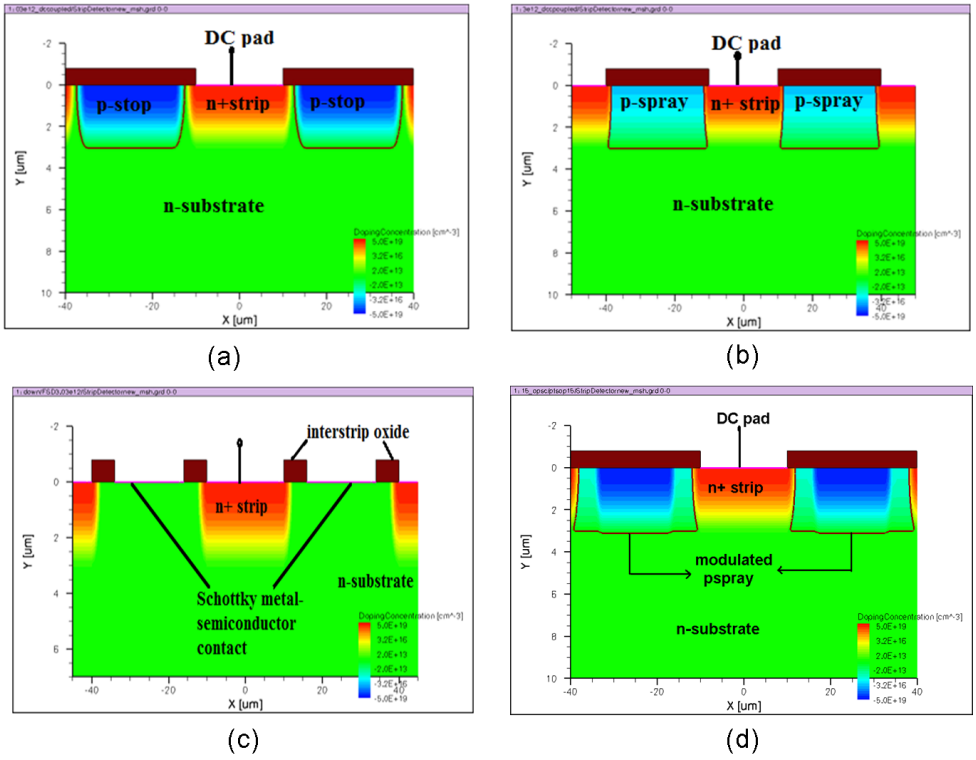

Figure 2: Simulated TCAD grid of DSSD having four different isolation techniques (a) P-stop; (b) P-spray; (c) Schottky barrier; (d) Modulated P-spray.

When high-energy particles such as hadrons pass through a detector, they collide with silicon atoms and displace them from their lattice sites, resulting in pairs of interstitial atoms and vacancies. These defects may recombine, or they may form complexes with each other or with existing impurities in the silicon [15, 16, 17]. These defects introduce extra energy levels within the bandgap of the silicon. SYNOPSYS simulates this bulk radiation damage by directly modelling the dynamics of these traps [18]. So, the user has to provide SYNOPSYS with the concentrations and parameters of the traps. The trap model used here is based on the work done at the University of Perugia [19].

Table 2: Comparison of measured and simulated data for irradiated DSSDs

Fluence n_{eq} cm^{-2}	Leakage Current @ 20^0C (nA)		V_{fd} (V)	
	Measured	Simulated	Measured	Simulated
2.06×10^{12}	5.4×10^{3}	5.68×10^{3}	47±5	45
3.03×10^{12}	9.5×10^{3}	8.31×10^{3}	29±5	37
3.93×10^{12}	10.7×10^{3}	10.7×10^{3}	29 ± 5	32
11.20×10^{12}	35.1×10^{3}	30.3×10^{3}	9 ± 5	9
20.60×10^{12}	66.5×10^{3}	58.8×10^{3}	50 ± 5	48

3. Results and discussion

3.1. Leakage current and depletion behaviour of sensors

Current-Voltage (I-V) characteristics were simulated for DSSDs and compared with measurements. In DSSDs, most of the bulk leakage current is due to electron-hole pairs being produced by Shockley-Read-Hall (SRH) gener-

Table 3: Expected power consumption of irradiated DSSDs

Fluence n_{eq} cm^{-2}	V_{op}(V)		Leakage Current @ -10^{0}C(nA)	R_{int}@ V_{op} (GΩ)		Power Consumption $V_{op} \times I_{leak}$ (μW mm^{-1})
	Measured	Simulated		Measured	Simulated	
3.03×10^{12}	60± 5	55	346	0.2± 0.05	1	8.10×10^{-2}
3.93×10^{12}	64 ± 5	62	448	0.1± 0.05	1.5	11.20×10^{-2}
11.20×10^{12}	8 ± 2	20	1250	0.1± 0.05	0.6	3.90×10^{-2}
20.60×10^{12}	120 ± 10	105	2420	0.1± 0.05	0.2	113.44×10^{-2}

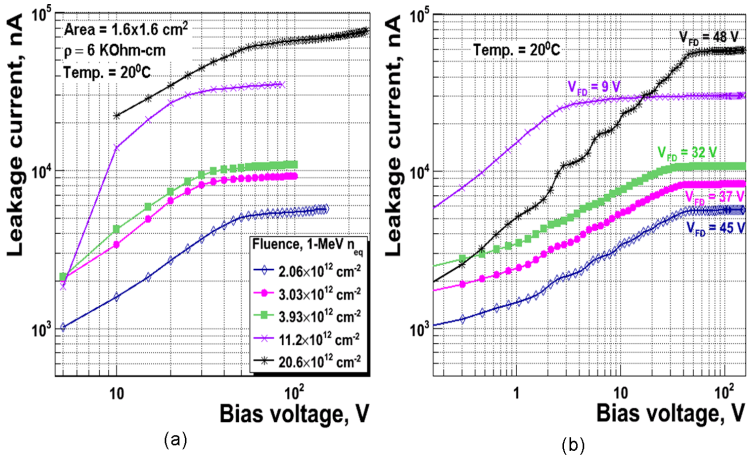

Figure 3: Current-Voltage characterstics of irradiated DSSDs having P-stop isolation obtained through (a) measurements and (b) simulations.

ation [18] in the depletion region, which are then swept to the electrodes by the electric field. Some of the CBM prototype DSSDs have been irradiated with neutrons at KRI cyclotron facility in St. Petersburg, Russia. The irradiated data are shown in Figure 3(a). The full depletion voltage (V_{fd}) indicates that the type inversion occurs at around 11.20×10^{12} n_{eq}cm^{-2}. The full depletion voltage decreases with increasing fluence until the point of type inversion and after type inversion it starts increasing with fluence. The simulated I-V curve shown in Figure 3(b) matches qualitatively with the measured curves for the irradiated sensors. A comparison of measured parameters with the simulated values is shown in Table 2. The leakage current increases with fluence, thus increasing the shot noise component in the ENC calculations. However this can be controlled by operating the sensors at cryogenic temperatures. The extracted damage constant(α) from simulation is about 3.73×10^{-17} A cm^{-1} while from measurement is about 4.2×10^{-17} Acm^{-1}. A similar agreement has also been found for DSSDs having Schottky barrier both for unirradiated and for the irradiated ones including the effect of annealing as can be seen in the figures 4(a) and 4(b).

3.2. Series Capacitance and resistance of sensors

Series capacitance and series resistance (trace resistance) are the dominant factors contributing to the total ENC. The strip capacitance is the sum of the capacitance to the backplane and direct capacitance to the adjacent strips (interstrip capacitance). For small pitch microstrip detectors having 300 μm thickness, the interstrip capacitance (C_{int}) is expected to dominate over the backplane capacitance. We have used TCAD simulations to extract the C_{int} both before and after irradiation. Figure 5 shows the measured variation of ohmic side C_{int} versus bias voltage (V_{bias}) for non-irradiated DSSDs having P-spray isolation. Figure 6 shows the simulated variation of C_{int} versus V_{bias} for both P-stop and P-spray isolation. For both the cases, it has been found that C_{int} initially increases till the point of full depletion. After full depletion, there is a steep fall in C_{int} and then it saturates.

One can notice that there is a nice match between simulated and measured C_{int} especially after full depletion. Also it becomes clear that P-stop isolation gives lower capacitance as compared with P-spray isolation. We have simulated the expected variation of C_{int} versus V_{bias} for Schottky barrier isolation in order to compare it with the conventional

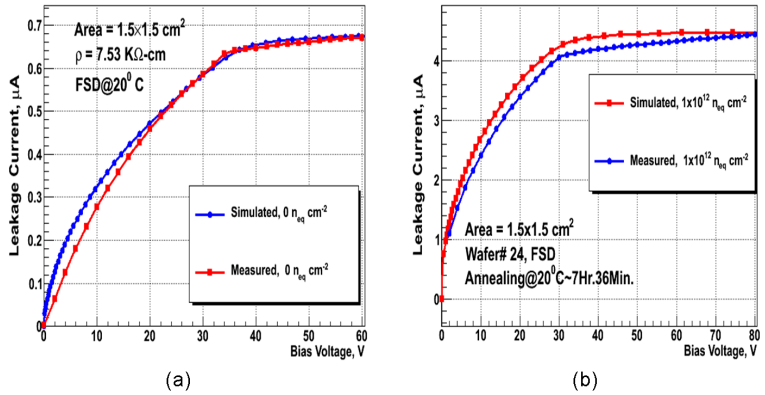

Figure 4: Comparison of measured variation of leakage current vs. bias voltage with simulation for DSSDs having schottky barrier isolation (a) at Zero fluence and (b) after irradiation with 1×10^{12} $n_{eq}cm^{-2}$.

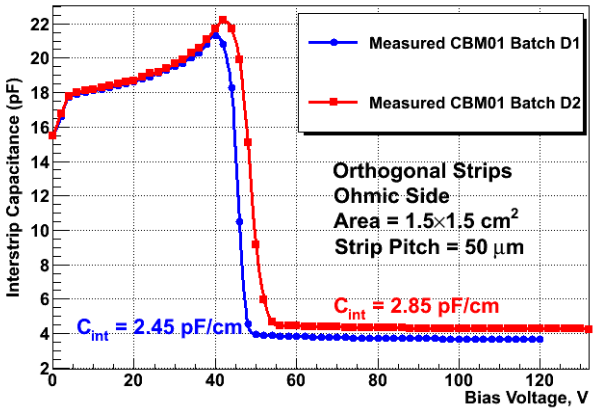

Figure 5: Measured variation of C_{int} with bias voltage for DSSDs having P-spray isolation.

isolation techniques. It is clear from Figure 7 that C_{int} for Schottky barrier isolation is slightly lower as compared with P-stop isolation technique after full depletion. However before full depletion, C_{int} for Schottky barrier isolation is too high both for unirradiated as also for irradiated DSSDs which could be detrimental if the DSSDs have to be operated under-depleted at high fluences. We wanted to study if there is an impact of irradiation on the interstrip capacitance. For this purpose, we have used our radiation damage model which has already been validated with measurements. Figure 8 shows the simulated variation of ohmic side C_{int} versus V_{bias} after irradiation for DSSDs equipped with P-stop. The shape of the C_{int} remains the same as for non-irradiated case. We do not observe a drastic change in the value of C_{int} with irradiation. It can be noted that the value of C_{int} before full depletion initially decreases with fluence till the point of type-inversion and increase thereafter. Figure 9 shows the variation of metal trace resistance as a function of frequency. The measured resistance has been found to be around 21 Ωcm^{-1}. The contribution from the parallel resistance to the ENC is negligible since it is inversely proportional to the value of bias resistor whose value is of order of few M Ω's.

3.3. Strip isolation and the charge collection efficiency

In order to investigate the life time of DSSDs, it is imperative to extract CCE as a function of fluence. One can understand strip isolation by studying interstrip resistance (R_{int}) in particular on the ohmic side. In figure 10(a),

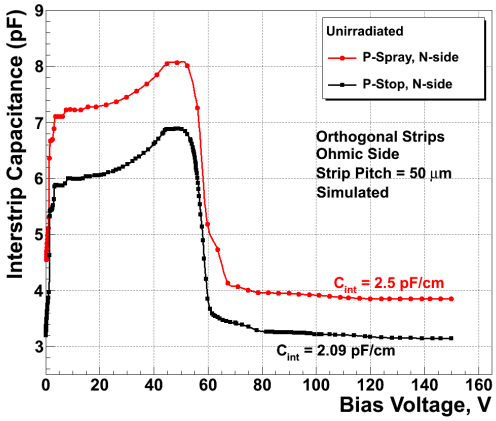

Figure 6: Simulated variation of C_{int} with bias voltage for DSSDs having P-spray and P-stop isolation.

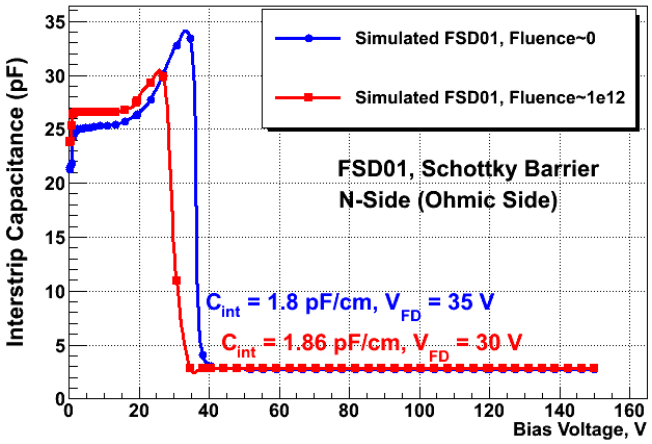

Figure 7: Simulated variation of C_{int} with bias voltage for DSSDs having Schottky barrier isolation.

the measured variation of ohmic side R_{int} with V_{bias} can be seen for different fluences. For the fluences up to type inversion, interstrip resistance is very low before full depletion and it increases steeply at full depletion and continues to increase slightly thereafter. However for type-inverted sensors, interstrip resistance is of the order of tens of MΩ's even before full depletion and saturates at around 100 MΩ after the operating voltage is reached. In type inverted sensors, this effect can be attributed to electron accumulation layer [20] due to which the type of silicon between the p-strips remains n-type as can be seen in Figure 11. To confirm this effect, e^- density between the p-strips has been extracted as shown in Figure 12. The high e^- density between p-strips confirm the presence of n-type substrate between the p-strips even after type-inversion. Thus, isolation on the p side is realized even at low biases after type inversion. Figure 10(b) shows the simulated values of interstrip resistance for the irradiated sensors for the same fluences as in measurements. A good match has been found for the fluences up to type inversion. However there is some discrepancy with the type inverted case for biases below full depletion. The simulated trap model is not able to reproduce the effect of electron accumulation layer in R_{int} simulation. Though this effect is reflected accurately in the transient simulations as discussed below. Also it should be noted from Figure 10(b) that the operating voltage is around 1.5-2.0 times the V_{fd} depending on the fluence. It is advisable to reduce the operating voltage since it directly increases the power consumption. Table 3 shows the expected power consumption of DSSDs irradiated up to

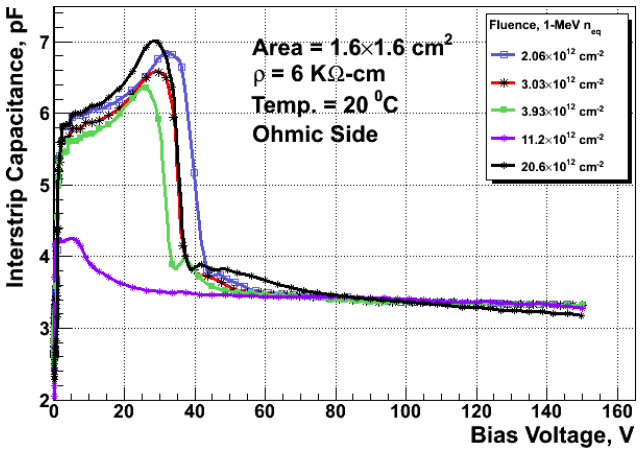

Figure 8: Interstrip capacitance vs. bias voltage for irradiated DSSDs equipped with P-stop isolation technique.

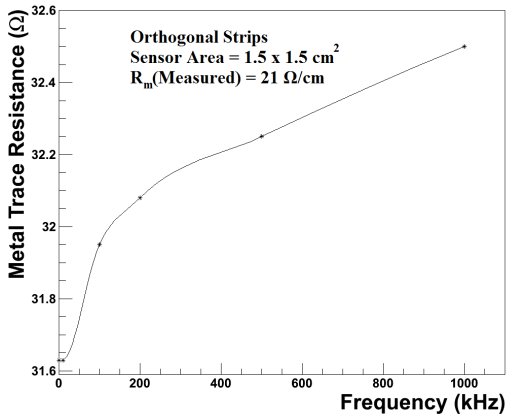

Figure 9: Measured trace resistance vs. frequency for DSSD equipped with P-spray isolation technique.

2.06×10^{13} $n_{eq}cm^{-2}$. One can observe that the power consumption increases steeply after type-inversion.

We have studied the charge collection through transient simulations by shooting a Minimum Ionizing particle (MIP) orthogonally on one of the junction side strips and observing the charge collection on the corresponding ohmic side strip. Figures 13(a) and 13(b) show the transient signals observed on the p-side of DSSD exposed to a fluence of 3.93×10^{12} $n_{eq}cm^{-2}$ and 20.60×10^{12} $n_{eq}cm^{-2}$ respectively. One can infer from these plots that the charge collection time in either case can be improved by operating the sensors at high bias voltage since in either case less mobile holes are being collected which can be confirmed from the polarity of the signal. Figure 14(a) and 14(b) show the transient signals observed on the n-side of DSSD exposed to a fluence of 3.93×10^{12} $n_{eq}cm^{-2}$ and 20.60×10^{12} $n_{eq}cm^{-2}$ respectively. It can be noted that for this case, charge collection is much faster as n-side is collecting electrons. These transient signals have been integrated over time to extract the collected charge.

In order to validate the transient simulations, we have reproduced the experimentally observed CCE for thin (140 μm) and thick (300 μm) n-in-p detectors irradiated to a fluence of 5.0×10^{14} $n_{eq}cm^{-2}$. The structure and substrate doping of the simulated device matched with those tested in Ref. [21]. The comparison of the simulated CCE with the measurements can be seen in Figure 15. The simulation results agree with measurements within 10 % error thus validating the transient simulations.

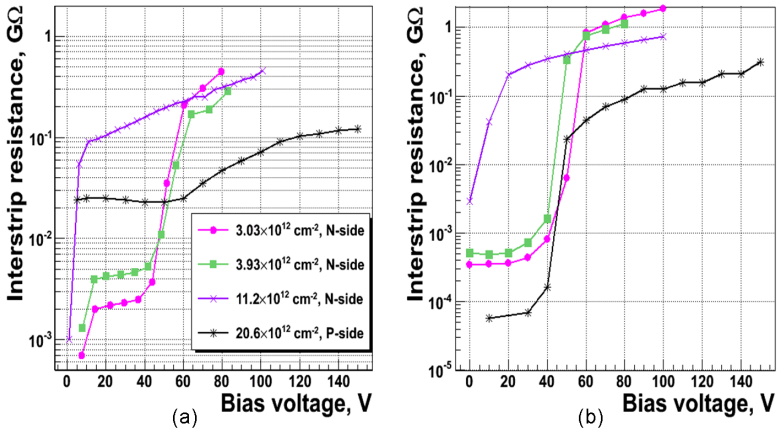

Figure 10: Variation of interstrip resistance vs. bias voltage of irradiated DSSDs having P-stop isolation technique obtained through (a) measurements and (b) simulations.

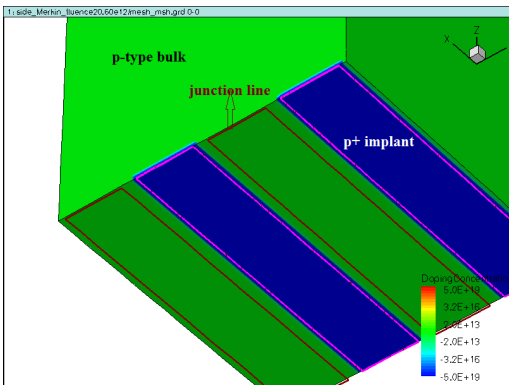

Figure 11: Junction line formed by type-inverted bulk and e^- accumulation layer on the ohmic side.

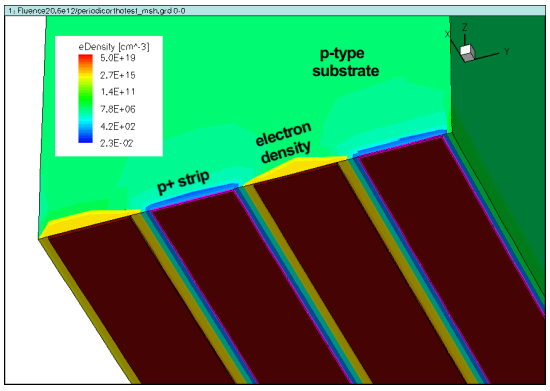

Figure 12: Electron density between the P-strips in type-inverted DSSD.

Figure 16 shows the variation of collected charge versus V_{bias} for the same fluences as used for irradiation. The

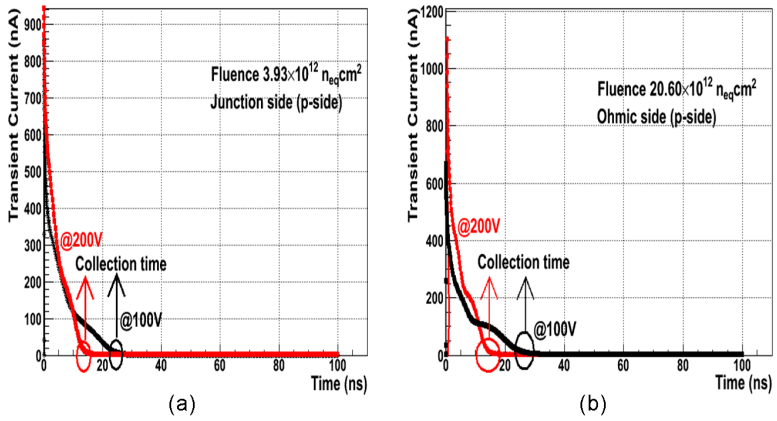

Figure 13: Transient signal on the p-side at V_{bias} 100V & 200V for DSSDs irradiated to (a) 3.93×10^{12} $n_{eq}cm^{-2}$ and (b) 20.60×10^{12} $n_{eq}cm^{-2}$.

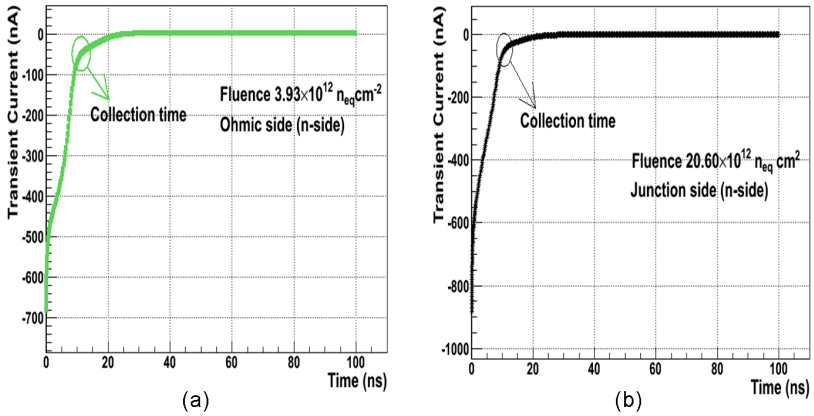

Figure 14: Transient signal on the n-side at V_{bias} 100V for DSSD irradiated to (a) 3.93×10^{12} $n_{eq}cm^{-2}$ and (b) 20.60×10^{12} $n_{eq}cm^{-2}$.

charge collection follows the same variation as measured R_{int} does with V_{bias}. Figure 17 shows the charge pickup (crosstalk) by neighbouring strip on the ohmic side as a function of V_{bias} . As expected, the crosstalk initially increases with V_{bias} for all the fluences since the depletion region gets wider, and so the amount of charge sharing between the neighbouring strips will increase. On the other hand, increasing the bias will also improve the drift velocity, which tends to reduce charge sharing. So, as the detector nears full depletion, this second effect becomes more important, and the crosstalk slowly decreases. It becomes clear from Figures 16 and 17 that the main impact of irradiation is the deterioration of CCE. We have tried to extract a mathematical model for the dependence of CCE on the carrier life time as can be seen in Figure 18.

3.4. Design optimization of isolation techniques in DSSDs

Table 4 shows the expected breakdown voltage (V_{bd}) for DSSDs exposed to a low fluence (before type-inversion) and high fluence (after type-inversion) having three isolation techniques namely P-stop, P-spray and Schottky barrier. The CBM plans to use floating electronics [22], hence for V_{bd} simulations, DC coupled DSSDs have been considered. One can notice that in all the three cases, the V_{bd} deteriorates with fluence. For DSSDs having conventional isolation

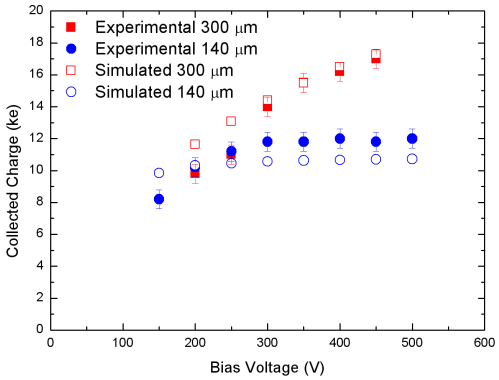

Figure 15: Comparison of measured CCE for thin and thick n-in-p detectors with transient simulations.

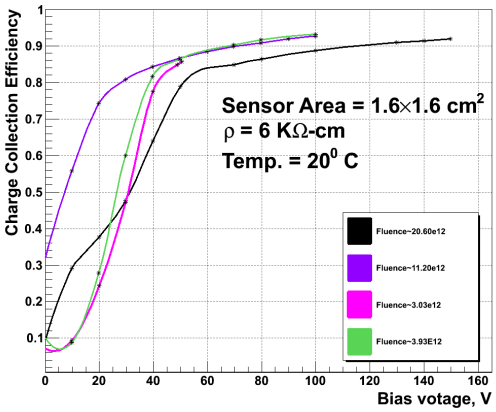

Figure 16: CCE versus bias voltage for irradiated DSSDs equipped with P-stop isolation.

techniques, this happens since before type-inversion the electric field is distributed on either sides while after type-inversion the high electric field exists only on the n- side. This can be seen from the Figure 19 . However in the case of DSSDs having Schottky barrier, the critical electric field responsible for breakdown occurs in the oxide between n-strips and schottky contact as can be seen from Figure 20. Hence the V_{bd} deteriorates with fluence since there is an increase in surface oxide charge with fluence. One can infer from Table 4 that in terms of breakdown performance, the Schottky barrier is the best choice.

Interstrip capacitance (C_{int}) has been simulated for DSSDs having conventional isolation techniques and also for DSSDs equipped with Schottky barrier both for low and high fluences as can be seen from Table 4. One can notice that the C_{int} on the p-side is lower as compared with n-side for DSSDs equipped with P-stop and P-spray. This again can be explained based on e^- accumulation layer [20] which helps in coupling the n-strips while doing an opposite effect between the p-strips. Also one can notice that with increasing fluence, the C_{int} on the p-side increases in larger proportion as compared with n-side. This could be explained since the silicon bulk inverts to P-type at higher fluence, which helps to overcome the inhibition of hole density by the electron accumulation layer between the p-strips. In the case of DSSDs having schottky barrier, a steep rise in the value of C_{int} is observed after type-inversion on the p-side. This has also been observed during measurements. Since the C_{int} on the p-side of DSSDs having schottky barrier is

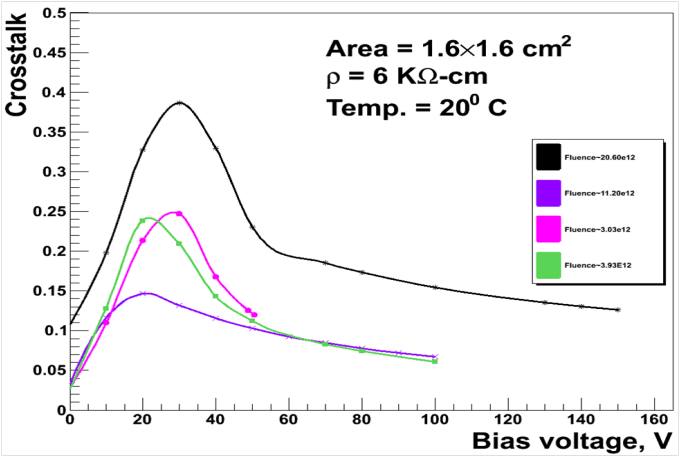

Figure 17: Cross-talk versus bias voltage for irradiated DSSDs equipped with P-stop isolation.

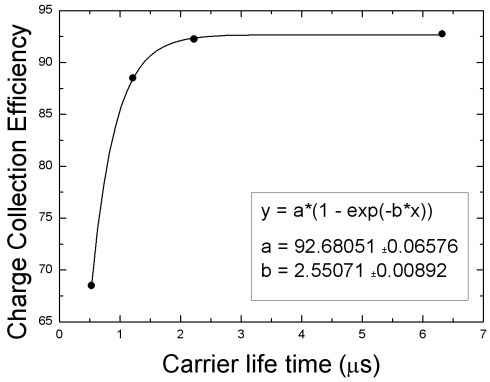

Figure 18: Modelling of dependence of CCE on carrier life time.

Table 4: Comparison of conventional isolation techniques with schottky barrier isolation in terms of static and dynamic parameters.

Isolation Technique	Fluence (n_{eq} cm^{-2})	V_{bd} (V)	C_{int} (pF cm^{-1})		R_{int} @ 80V (MΩ)	CCE @ 80V %
			n-side	p-side		
P-spray	3.93×10^{12}	524	2.6	1.7	1250	93
	20.60×10^{12}	450	2.7	2.1	104	86.25
P-stop	3.93×10^{12}	860	2.1	1.7	1136	91.25
	20.60×10^{12}	750	2.29	2.1	125	86.25
Schotkky Barrier	3.93×10^{12}	1450	2.05	1.7	19.64	79
	20.60×10^{12}	1350	1.8	4.0	8	77.5

too high at high fluence, this is not a good choice for isolation technique in terms of capacitive noise.

Figure 21 shows the variation of R_{int} versus V_{bias} for DSSDs equipped with P-stop, P-spray and Schottky barrier at low and high fluences. One can observe that for low fluence, P-spray gives better isolation as compared with P-stop. The operating voltage with P-spray isolation technique is reached at 35 V while with P-stop, the operating voltage

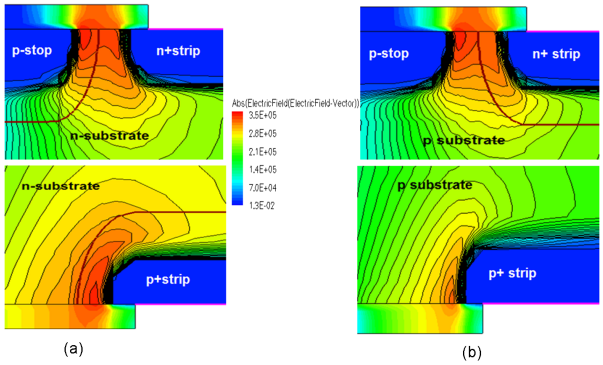

Figure 19: Simulated electric field distribution on n and p side of the DSSD at breakdown irradiated to a fluence of (a) 3.93×10^{12} $n_{eq}cm^{-2}$ (before type-inversion) and (b) 20.60×10^{12} $n_{eq}cm^{-2}$ (beyond type-inversion).

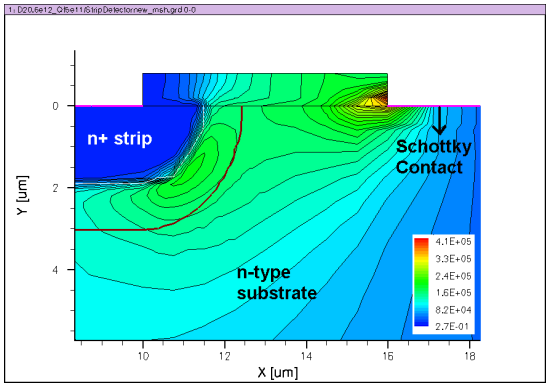

Figure 20: Simulated electric field distribution at breakdown for DSSD equipped with schottky barrier.

Table 5: Optimization of modulated p-spray

p-spray dose (cm^{-3})	1×10^{15} (very low dose)			4×10^{16} (low dose)			8×10^{16} (medium dose)			12×10^{16} (high dose)		
p-stop width (μm)	V_{bd}(V)	C_{int}(pF cm^{-1})		V_{bd}(V)	C_{int}(pF cm^{-1})		V_{bd} (V)	C_{int}(pF cm^{-1})		V_{bd} (V)	C_{int}(pF cm^{-1})	
		n-side	p-side		n-side	p-side		n-side	p-side		n-side	p-side
5	1125	1.56	1.75	490	2.405	1.75	210	2.46	1.76	161	2.47	1.77
10	1125	1.5	1.75	480	2.4	1.75	205	2.46	1.76	160	2.47	1.77
15	1150	1.6	1.75	488	2.37	1.75	205	2.43	1.76	160	2.47	1.77
20	650	2.09	1.75	450	2.51	1.75	205	2.42	1.76	160	2.47	1.77

is at 45 V. The R_{int} for DSSD with schottky barrier is comparatively very low and its operating voltage is reached at 90 V. For high fluence, the R_{int} of P-spray and P-stop are almost same and both reach their operating voltage at around 70V. Again for DSSD having schottky barrier, R_{int} is throughout low and the operating voltage is reached at 100 V. As discussed in Section 3.3, higher operating voltage means higher power consumption which could lead to thermal runaway at high fluences. Figure 22 shows the variation of CCE versus V_{bias} for DSSDs having conventional isolation techniques and schottky barrier. Again the CCE mimics the variation of R_{int} with V_{bias}. For low fluence, P-spray gives better CCE as compared with P-stop while Schottky barrier gives the worst performance in terms of CCE. As in the case of R_{int}, at high fluence, the CCE of P-stop and P-spray is same while for schottky barrier, the CCE is very poor. Hence in terms of power consumption and CCE, it seems not optimal to use Schottky barrier as an effective isolation

Table 6: Comparison between p-stop, p-spray and optimized modulated p-spray at low and high fluence.

Isolation Technique	Fluence (n_{eq} cm^{-2})	V_{bd} (V)	C_{int} (pF cm^{-1})	CCE %
P-stop	2×10^{13}	800	2.08	93.15
	1×10^{14}	610	2.09	88.87
P-spray	2×10^{13}	513	2.56	93.17
	1×10^{14}	495	2.44	89
Optimized Modulated P-spray	2×10^{13}	1600	1.58	93.22
	1×10^{14}	1150	1.60	89

technique.

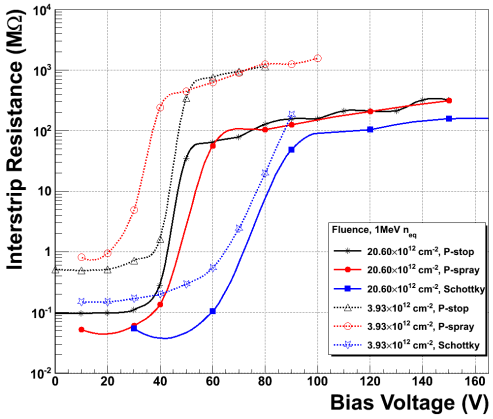

Figure 21: Comparison of R_{int} vs. V_{bias} for DSSDs equipped with P-stop, P-spray and Schottky barrier at low and high fluences.

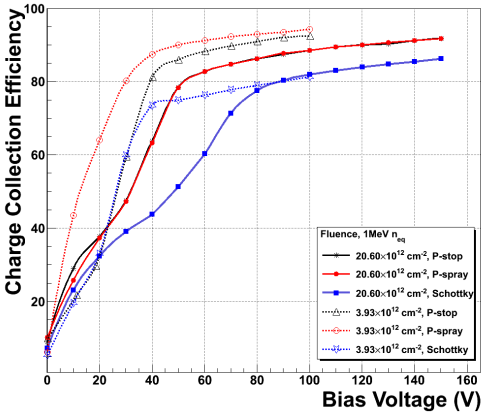

Figure 22: Comparison of CCE vs. V_{bias} for DSSDs equipped with P-stop, P-spray and Schottky barrier at low and high fluences.

An optimization study has been done for modulated P-spray in terms of P-spray dose and P-stop width for the maximum expected fluence of 1×10^{14} n_{eq}cm^{-2}. It is known that narrow P-stop improves the V_{bd} but deteriorates the

C_{int} [23, 24] while in the case of P-spray, higher dose implies premature breakdown and higher C_{int} for the p-type substrate. We have taken various combinations of P-stop width and P-spray dose and extracted the V_{bd} and C_{int}. As can be seen from Table 5, the C_{int} increases and V_{bd} decreases with P-spray dose for a fixed P-stop width. Also, one can observe from Table 5 that for a fixed P-spray dose, the V_{bd} initially increases with P-stop width till 15 μm but deteriorates afterwards. This effect is more prominent for very low and low P-spray dose. From this table, it becomes clear that the best design criteria is to combine very low P-spray dose (1×10^{15} cm^{-3}) with 15 μm P-stop width, referred to as Optimized Modulated P-spray in Table 6 . Finally a comparison of P-stop, P-spray and Optimized Modulated P-spray for 1^{st} year of CBM run fluence (2×10^{13} n_{eq}cm^{-2}) and the maximum fluence expected at the end of five years of CBM run (1×10^{14} n_{eq}cm^{-2}) has been shown in Table 6. It is clear from this table that optimized modulated P-spray is the best choice for isolation technique in terms of V_{bd}, C_{int} and CCE.

4. Conclusions

This paper reports on the ongoing R&D effort to develop radiation hard low noise radiation hard DSSDs for the upcoming CBM experiment at FAIR. An optimization of isolation techniques has been done to maximize CCE and V_{bd} while minimizing the total ENC. Transient simulations has proven to be an effective tool to determine the operating voltage and to predict the expected CCE.

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